ABSTRACT OF THE DISCLOSURE

A system and a method capable of automatically reading out the multiple value of clock frequency on system bus are provided. The system includes a central processing unit and a chipset. The central processing unit has a storage unit for holding a multiple value of clock frequency. The storage unit is capable of synchronizing with an external device through a serial initialization packet (SIP) protocol. The chipset attempts to synchronize with the central processing unit in a SIP protocol that uses a preset multiple value of clock frequency as a parameter. If synchronization between the central processing unit and the chipset cannot be established, the preset multiple value of clock frequency is changed and the SIP protocol is executed again. The multiple value of clock frequency is reset until synchronization is established. After synchronization, the multiple value of clock frequency in the central processing unit is retrieved and compared with the preset multiple value of clock frequency. If the retrieved multiple value of clock frequency is different from the preset value in the chipset, the preset value is replaced by the retrieved value.